REMARKS

This response responds to the Office Action dated October 13, 2004 in which the Examiner rejected claims 1-9 under 35 U.S.C. §102(b).

Claim 1 claims a semiconductor storage device comprising a nonvolatile memory to which data is written in a sector unit, and a data rewriting unit rewriting data in the nonvolatile memory. Each sector in the nonvolatile memory includes: a data area into which data is stored; and a refresh mark into which information indicative of whether refresh has been performed or not is stored. The data rewriting unit includes a refresh execution unit referring to the refresh mark and determining whether the sector is refreshed or not, thereby executing the refresh.

Through the structure of the claimed invention having a refresh mark which indicates whether a refresh has been performed, as claimed in claim 1, the claimed invention provides a semiconductor storage device which eliminates the need for a refresh counter and prevents the concentration of writing/erasing. The prior art does not show, teach or suggest the invention as claimed in claim 1.

Claims 1-9 were rejected under 35 U.S.C. §102(b) as being anticipated by *So et al* (U.S. Patent No. 6,151,246).

Applicant respectfully traverses the Examiner's rejection of the claims under 35 U.S.C. §102(b). The claims have been reviewed in light of the specification, and for reasons which are set forth below, Applicant respectfully requests the Examiner withdraws the rejection to the claims and allows the claims to issue.

So et al appears to disclose a typical flash memory architecture which erases a sector as a unit and does not provide a mechanism for erasing or reducing the threshold voltage of individual memory cells. In such flash architectures, a sector

containing a data error can be marked as requiring a refresh. Special memory cells in the array or a separate register can be used to identify the data sectors marked for a refresh. FIG. 6 illustrates a system 600 capable of performing scheduled or delayed refreshes of sectors. In system 600, an error detection circuit 655 detects data errors in data that a read circuit 650 reads from memory array 140. Error detection can occur as described above when a read circuit 650 reads a memory cell having a threshold voltage in a forbidden zone or as described below when a data value read is inconsistent with an error detection and correction code. When an error is detected, error detection circuit 655 marks the sector as requiring a refresh, for example by directing read/write control 670 to write a flag value in overhead memory cells in the sector containing the data error or write a sector number in a register in a refresh control 620. The refresh for a data sector marked as containing a data error need not be immediate. Instead refresh control 620 can wait for a period of inactivity of memory 600 before initiating a refresh operation on the marked sector. Alternatively, if the flag is stored in non-volatile memory, the refresh operation can occur during a start up procedure in which refresh control 620 checks for sectors requiring a refresh operation. (Col. 8, line 45 through Col. 9, line 5)

Thus, *So et al* merely discloses special cells in an array used to identify the data sectors marked for a refresh (col. 8, lines 50-52) and a detection circuit 655 which marks a section requiring a refresh (col. 8, lines 60-65). Nothing in *So et al* shows, teaches or suggests a refresh mark which indicates whether refresh has been performed as claimed in claim 1. Rather, *So et al* merely discloses an overhead memory cell which stores a flag value indicating a refresh is required.

Since nothing in *So et al* shows, teaches or suggests a refresh mark which indicates whether refresh has been performed as claimed in claim 1, applicant respectfully requests the Examiner withdraws the rejection to claim 1 under 35 U.S.C. §102(b).

Claims 2-9 depend from claim 1 and recite additional features. Applicant respectfully submits that claims 2-9 would not have been anticipated by *So et al* within the meaning of 35 U.S.C. §102(b) at least for the reasons as set forth above. Therefore, applicant respectfully requests the Examiner withdraws the rejection to claims under 35 U.S.C. §102(b).

The prior art of record, which is not relied upon, is acknowledged. The references taken singularly or in combination do not anticipate or make obvious the claimed invention.

Thus it now appears that the application is in condition for reconsideration and allowance. Reconsideration and allowance at an early date are respectfully requested.

If for any reason the Examiner feels that the application is not now in condition for allowance, the Examiner is respectfully requested to contact, by telephone, the applicant's undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed within the currently set shortened statutory period, applicant respectfully petitions for an appropriate extension of time.

The fees for such extension of time may be charged to our Deposit Account No. 02-4800.

In the event that any additional fees are due with this paper, please charge our Deposit Account No. 02-4800.

Respectfully submitted,

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